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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
JRL-550-534

Application Number	Filed
10/802,032	March 17, 2004
First Named Inventor: NIGHTINGALE	
Art Unit: 2123	Examiner: Janakiraman, Nithya

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____


Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

October 19, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and selection option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

NIGHTINGALE, A. et al.

Atty. Ref.: 550-534; Confirmation No. 8029

Appl. No. 10/802,032

TC/A.U. 2123

Filed: March 17, 2004

Examiner: Janakiraman, Nithya

For: DATA PROCESSING APPARATUS SIMULATION

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October 19, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

The claims are concerned with simulating the operation of a data processing apparatus to determine timing information of data transfers. The inventors recognized that during the operation of many data processing apparatus, the probability that a data transfer will occur between a master and slave pair over the bus without the bus being requested for use by other pairs is statistically relatively high. Hence, for the majority of data transfers, it is accurate to assume that the data transfer will occur with exclusive access to the bus. Operating on that assumption provides many benefits including significantly decreased complexity, increased speed, and increased accuracy when generating the anticipated timing information for each data transfer. If the anticipated timing information indicates that more than one data transfer will occur on the bus at the same time, it is then assumed that the anticipated timing information is inaccurate and revised timing information is then generated, which is only in a minority of the data transfers.

All claims are rejected based on Fischer, Thekkath, and Best. Fischer describes an asynchronous network that adjusts the timing of data transmission so as to adapt to the network load. This adjustment takes place for future transactions based upon the result of preceding transactions. The Examiner appears to be using Best to teach multiple bus masters and multiple bus slaves missing from Fischer. The Examiner also admits that Fischer does not simulate the master-slave transaction or compensate for two or more concurrent transactions. The Examiner relies on a third reference to Thekkath, which discloses a bus arbiter.

Clear Error #1: Thekkath does not describe a specific simulation methodology.

Claim 1 recites a "method of simulating the operation of a data processing apparatus to determine timing information of data transfers" and then three specific steps (a)-(c) to that method. The Examiner suggests that Thekkath discloses simulating the bus/master device referring to col. 6, line 57-col. 7, line 5. Nothing in this text says anything about simulation. The text at col. 5, lines 29-31 uses the words "for use in...simulating...an integrated bus device." But this does not teach a specific simulation technique. Instead, information describing the hardware design of Thekkath is provided which could then be subject to simulation by some other system. See col. 5, lines 31-37. But Thekkath gives no information as to how such simulation is actually performed. This general, "intended use" statement in Thekkath and the Examiner's general characterization of a "simulation computer program" on page 2 of the FOA fail to teach the specific simulation steps recited in claim 1.

Clear Error #2: Missing claim feature: generating anticipated timing information by assuming that each data transfer will occur with exclusive access to the bus.

All the references lack step (a) of claim 1. The Examiner cites [0012] of Fischer for this feature. But there is no teaching in [0012] where it is assumed that data transfer will occur with exclusive access to the bus. Fischer may determine timing information, but this is not timing

information based upon a specified assumption of exclusive bus access as specified in the claims. Fischer operates at a much higher statistical level than individual data bus transfers.

In Thekkath, the bus arbiter ensures that each bus transaction in Thekkath will have exclusive access to the bus. As a result, there is no need in Thekkath for anticipated timing information or any assumption that data transfers will occur with exclusive access to the bus because the arbiter ensures exclusive bus access. Precluding bus contentions using an arbiter is not the same as "generating anticipated timing information for each successive data transfer over the bus by assuming that each successive data transfer can occur with exclusive access to the bus." If such an assumption were made in Thekkah, what role would Thekkah's arbiter play?

Clear Error #3: Missing claim feature: determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus.

All the references lack step (b) of claim 1. The Examiner cites col. 5, lines 1-10 of Thekkath as disclosing "detecting what would be the capability of the bus." The Examiner complains in the final action that this quote is not in the claim. But that was not argued. Instead, Applicants addressed this quoted language because it was and is used by the Examiner in rejecting step (b). Col. 5, lines 1-10 state that the "slave configuration logic stores a burst transaction capability corresponding to the slave device." The burst transaction capability is a capability of the slave device—not the bus. See also col. 5, lines 6-7. The point is that contrary to the Examiner's contention, Thekkath does not detect a capability of the bus. Nor would detecting a capability of the bus be the same thing as determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus.

Thekkath's bus arbitration logic 104 simply determines whether transaction requests have been received from initiating devices and grants or refuse requests according to an arbitration algorithm. Col. 7, lines 1-31. The arbiter itself does not anticipate actual concurrent transfers on

the bus. The Examiner fails to shows where Thekkath's arbiter determines anticipated timing information associated with the requests to determine whether two or more concurrent data transfers would occur on the bus. Instead, the arbiter simply prevents concurrent data transfers.

Clear Error #4: Missing claim feature: "generating machine-readable revised timing information for those data transfers for use in correcting said anticipated timing information as part of simulation output results."

All the references lack step (c) of claim 1. The Examiner asserts that "Fischer teaches that continuous revisions take place to adjust for the transaction interference, or errors, of Thekkath in paragraph 0012 [of Fischer]. However, Fischer's continuous slave node clock correction is not a correction of timing information. The slave node clock is a clock signal that controls operation of the slave device. The slave node clock is not timing information for the claimed concurrent data transfers. Fischer does not revise anticipated timing information for concurrent data transfers because Fischer's clock correction is at a much higher statistical level than at the individual bus conflict level.

Clear Error #5: The Combination of Fischer or Thekkath Is Improper.

There is no reasonable basis to use a technique for arbitrating requests for transfers on an internal system bus in communications between separate nodes externally connected by a network. Fischer's communications network will typically have many thousands of terminals (see the many houses in Figure 1c of Fischer) with fiber optic cables being used so that multiple data transfers can be carried across the network at the same time. The Examiner admits that Fischer does not compensate for two or more concurrent transactions. The reason Fischer does not do such compensation is that preventing two or more concurrent transactions would result in thousands of people being cut off from the network every time a single person uses the network, which would not be sensible. Given that such exclusive access to the network is undesirable in

Fischer, the skilled person would not introduce a Thekkah's bus arbiter into the network in order to enforce exclusive network access.

The Examiner argues the combination "because it is desirable to test and simulate for 'a burst data transaction to be optimized ...for efficient transfer over a bus'" and because having two devices transfer data on the bus at the same time precludes any transfer of data. Following the Examiner's motivation in this case, the bus arbiter of Thekkath would be modeled so that bus contention is prevented from ever occurring at the expense of a slower and more complex simulation. Thus, the combination proposed by the Examiner is one in which there would be no generation of anticipated timing information or correction of that anticipated timing information because with the Examiner's combination the modeled bus arbiter ensures that no correction is necessary. But the proposed combination which uses a bus arbiter is not what is claimed.

Accordingly, the obviousness rejection of claims 1-46 based on Fischer, Thekkath, and Best should be withdrawn and the case allowed.

Respectfully submitted,
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